1. A method to form a SRAM memory cell in an integrated circuit device comprising:

providing a bi-stable flip-flop cell having a data storage node and a data bar storage node; and

forming a first capacitor coupled to said data bar storage node and a second capacitor coupled to said data storage node wherein said first and second capacitors comprise a first conductor layer overlying a second conductor layer with a dielectric layer therebetween and wherein one of said first and second conductor layers is coupled to ground.

2. The method according to Claim 1 wherein said bi-stable flip-flop cell comprises two pull-up transistors, two pull-down transistors, and two pass transistors.

3. The method according to Claim 1 wherein said first and second conductor layers comprise polysilicon.

4. The method according to Claim 1 wherein said first and second conductor layers comprise metal and wherein one of said first and second metal layers comprises a standard metal level in said integrated circuit device.

5. The method according to Claim 1 wherein one of said first and second conductor layers comprises metal nitride.

6. The method according to Claim 1 wherein said dielectric layer comprises nitride.

7. The method according to Claim 1 wherein said dielectric layer comprises metal oxide.

8. The method according to Claim 1 wherein said first and second capacitors are formed by a method comprising:

depositing said dielectric layer overlying said first conductor layer;

depositing said second conductor layer overlying said dielectric layer;

defining a capacitor mask overlying said second conductor layer in planned capacitor areas; and

removing said second conductor layer and said dielectric layer from all areas not covered by said capacitor mask.

9. A method to form a SRAM memory cell in an integrated circuit device comprising:

providing a bi-stable flip-flop cell having a data storage node and a data bar storage node; and

forming a first capacitor coupled to said data bar storage node and a second capacitor coupled to said data storage node wherein said first and second capacitors comprise a first metal layer overlying a second metal layer with a dielectric layer therebetween, wherein one of said first and second metal layers is coupled to ground, and wherein said first and second capacitors are formed by a method comprising:

depositing said dielectric layer overlying said first metal layer;

depositing said second metal layer cverlying said dielectric layer;

defining a capacitor mask overlying planned capacitor areas; and

removing said second metal layer and said dielectric layer from all areas not covered by said capacitor mask.

10. The method according to Claim 9 wherein said bi-stable flip-flop cell comprises two pull-up transistors, two pull-down transistors, and two pass transistors.

11. The method according to Claim 9 wherein said first metal layer comprises a standard metal level in said integrated circuit device.

12. The method according to Claim 9 wherein said dielectric layer comprises nitride.

13. The method according to Claim 9 wherein said dielectric layer comprises a metal oxide.

14. A SRAM memory cell in an integrated circuit device comprising:

a bi-stable flip-flop cell having a data storage node and a data bar storage node;

a first capacitor coupled to said data bar storage node and a second capacitor coupled to said data storage node wherein said first and second capacitors comprises a first conductor layer overlying a second conductor layer with a dielectric layer therebetween and wherein one of said first and second conductor layers is coupled to ground.

15. The device according to Claim 14 wherein said bi-

stable flip-flop cell comprises two pull-up transistors, two pull-down transistors, and two pass transistors.

16. The device according to Claim 14 wherein said first and second conductor layers comprise polysilicon.

17. The device according to Claim 14 wherein said first and second conductor layers comprise metal and wherein one of said first and second conductor layers comprises a standard metal level in said integrated circuit device.

18. The device according to Claim 14 wherein said dielectric layer comprises nitride.

19. The device according to Claim 14 wherein said dielectric layer comprises a metal oxide.

20. The device according to Claim 14 wherein said second metal layer comprises metal nitride.